We Claim:

1. A circuit configuration for outputting bits of a data word in parallel, the configuration comprising:

a plurality of signal lines for providing data signals in parallel representing at least two bits of a data word, the data word including at least two bits;

a plurality of output terminals for providing amplified data signals representing the bits of the data word;

a control device having at least two outputs for outputting a respective control signal, said control device having at least two inputs connected to said signal lines, said control device for determining signal states of data signals representing bits of two directly successive data words on said plurality of signal lines;

a plurality of driver stages having inputs for obtaining the data signals from said plurality of signal lines, said plurality of driver stages having outputs connected to said plurality of output terminals; and

a plurality of additional driver stages, connected in parallel with said inputs and said outputs of said plurality of said driver stages, each one of said plurality of additional driver

stages connected in parallel with a respective one of said plurality of said driver stages;

said control device for generating a plurality of control signals for enabling or switching off said plurality of additional driver stages; and

each one of said plurality of said additional driver stages having an input connected to a respective one of said outputs of said control device for receiving one of said plurality of control signals generated by said control device.

2. The circuit configuration according to claim 1, wherein:

at each of said inputs of said control device, said control device is configured for determining signal state pairs comprised of a first data signal representing a bit of a data word and a second data signal representing a bit of an immediately successive data word; and

said signal state pairs include:

a rising edge of said first data signal followed by a falling edge of said second data signal, and

a falling edge of said first data signal followed by a rising edge of said second data signal.

3. The circuit configuration according to claim 2, wherein:

if said control device determines that two of said signal state pairs are simultaneously present, then said control device forwards a control signal to one of said plurality of additional driver stages assigned to one of said plurality of signal lines for which one of said signal state pairs has been determined;

if said control device determines that three of said signal state pairs are simultaneously present, then said control device forwards a respective control signal for two identical ones of said signal state pairs to ones of said plurality of additional driver stages assigned to ones of said plurality of signal lines for which said two identical ones of said signal state pairs have been determined; and

if said control device determines that more than three of said signal state pairs are simultaneously present, then said control device forwards a respective control signal to each of said plurality of additional driver stages assigned to ones of said plurality of signal lines for which one of said signal state pairs has been determined.

4. The circuit configuration according to claim 3, wherein said plurality of additional driver stages are driven directly before transferring a second bit of a signal state pair.

5. The circuit configuration according to claim 1, wherein each one of said plurality of additional driver stages is driven by a respective one of the data signals provided by said plurality of said signal lines and by a respective one of said plurality of control signals generated by said control device.